Microelectronics

ANADIGICS Shipments Pass 750m

ANADIGICS, Inc. said that total product shipments over its history recently passed the 750m unit mark. "We are extremely proud of this milestone, which demonstrates how technology leadership can be leveraged into product leadership," said Dr. Bami Bastani, President and CEO of ANADIGICS. "Whether it's a mobile handset using our HELP power amplifiers to achieve longer talk-time or CATV set-top box using our active splitters and multiple tuners to enable advanced PVR functionality, ANADIGICS' differentiated solutions are enabling manufacturers to evolve their products and meet the growing demands of tech-savvy consumers."
Web: www.anadigics.com

Mitsubishi InGaP HBT for WiMAX

Mitsubishi Electric Corp., high output InGaP HBT is to sample ship in December. The amplifiers are for WiMAX terminals used in mobile and domestic markets, and are the smallest of its kind in the industry. It developed the 4.5 mm amplifier by embedding the power detector (analyses the amplifier output) and step attenuator (controls amplifier output) in the module. The height has also been kept to 1 mm, so it can also be used in PC card terminals. The external matching circuit is also unnecessary because impedance of the input/output port is at the wireless device standard of 50 ohms. This reduces the number of parts and mounting area, and thus will reduce size and weight of the WiMAX terminal. The company plans to make an amplifier for 3.5 GHz and 2.3 GHz band by early fiscal 2008.
Web: global.mitsubishielectric.com

IEDM Showcase for IMEC Fin-FET

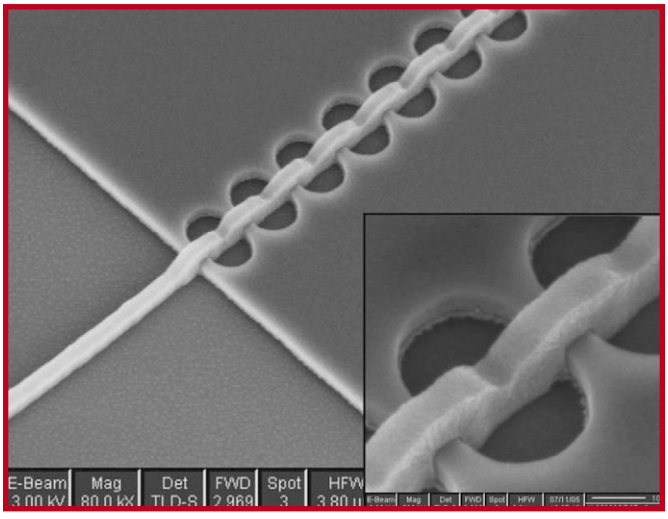
IMEC and its core partners will feature in 17 papers at the IEEE International Electron Devices Meeting (December 11–13, San Francisco). They claim this is a record in number of papers at a leading conference on semiconductor technologies. It showcases the success of IMEC's global R&D efforts to create solutions for (sub-)32 nm scaling.

Several advances will be reported in the scaling of logic technology options. For extending bulk CMOS into the 45/32 nm nodes, IMEC has developed an alternate integration process for their FUSI technology that is more manufacturing friendly without the need for a CMP (chemical mechanical polishing) step. It is based on using a planarizing resist and etch-back to open the FUSI gates.

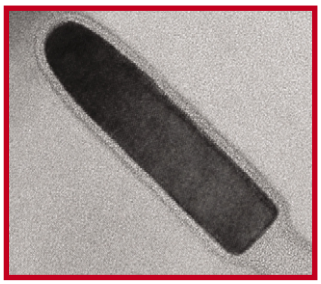
On the alternate metal gate option, *i.e.* metal-gate first approach or deposited metals, IMEC reports on MoOx as a promising pFET.

Two papers on FinFET CMOS will be reported demonstrating the impact of fin line-edge roughness on device characteristics, as well as the process technology to double or quadruple the fin density per area. Pioneered by TSMC, at the 2002 International Electron Devices Meeting, AMD announced the world's smallest double-gated FinFETs at the time, with 10 nm gates. IBM, Motorola and Intel have also published work in this area.

Beyond silicon as a substrate, IMEC will demonstrate a short channel Ge pMOS device built with Si-compatible process techniques. Reliability is an important factor in any semiconductor process development and forms an integral part of the technology development programs at IMEC. IMEC will present several results on reliability both in the field of 32 nm CMOS and flash memories. A detailed electrical and failure analysis of the impact of using Cu contacts on the CMOS front-end yield and reliability will be reported. For the first time, NBTI (negative biased temperature instability) degradation experiments under AC conditions at frequencies up to 2 GHz in SiON-based dielectrics will be presented. It will also be shown that ultra-fast progressive breakdown in HfO_2/TaN/TiN gate stacks n/p-MOSFETs only occurs during substrate injection, along with a model to explain this polarity dependence.



IMEC's 32nm Fin-FET.


IMEC's Fin-FET with polysilicon-SiOn gate stack.

Papers on non-volatile memory will focus on reliability modelling. A model that allows description of the leakage current through high-k insulators will be shown, which is essential to predict the long-term retention time for new-generation Flash technologies incorporating high-k interpoly dielectrics and/or tunnel layers. Also a consistent model for the description of the retention of localized charge trapping devices based on channel hot carrier injection into nitride layers will be presented.

"The results that will be presented at IEDM 2006 show that IMEC and its core partners have made significant advances in the fundamental understanding of bottlenecks in (sub-)32 nm scaling and developing the generic process steps, modules and devices," said Luc Van den hove, VP Silicon Process and Device Technology at IMEC. "We are excited that the combined effort of the IMEC research team and our core partners result in solutions for continued CMOS scaling feeding directly into development teams."

Besides results achieved in the (sub-)32 nm research platform, IMEC will also report a new integration process for backside thinned CMOS imagers with increased performance.

Web: www.imec.be